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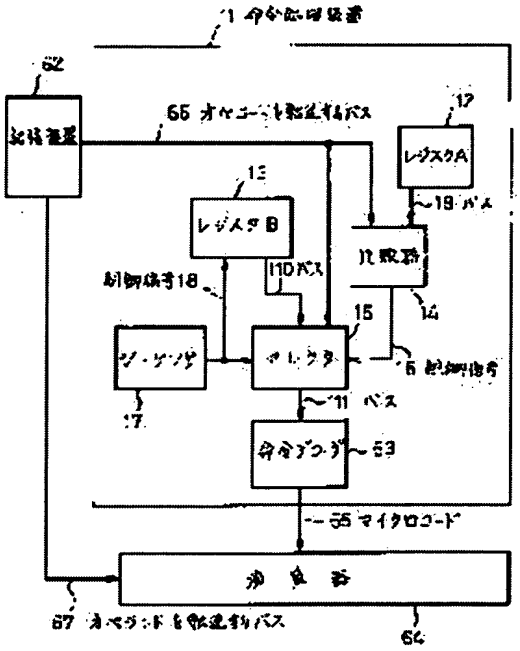
(54) TRANSLATION DEVICE, INFORMATION PROCESSOR AND RECORDING MEDIUM

(57)Abstract:
PROBLEM TO BE SOLVED: To provide an information processor, a translation device and their recording medium by which an operation code part of a short word length is assigned to an instruction high in usage frequency for every program without changing an instruction decoder.
SOLUTION: When an instruction map where a reservation area is secured in the instruction map is provided and the instruction with a long word length of the operation code part is used highly frequently, an operation code is replaced with that with a short code length which is previously reserved and the operation codes before and after the replacement are written in registers A12 and B13 so that the compression of an optimum code size is attained at every program without changing an instruction processor 11.



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* NOTICES *

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3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The translation equipment characterized by to have an assemble means is translation equipment which changes into the program of a machine instruction code the program written by the mnemonic, inputs an instruction of a mnemonic notation, and generate a corresponding machine instruction code, and the machine instruction code-generation means which transpose the 1st specific machine instruction code of the inside generated by said assemble means to the 2nd machine instruction code with the word length short than said 1st machine instruction code.
[Claim 2] Said translation equipment is translation equipment according to claim 1 characterized by searching the train of the machine instruction code generated by said assemble means, having a frequency analysis means to extract a machine instruction code with the high frequency of occurrence, and determining said 1st machine instruction code based on the result of the frequency analysis in said frequency analysis means.
[Claim 3] Said translation equipment An instruction read-out means, a decode means, and the 1st instruction maintenance means, A comparison means to detect coincidence with the 2nd instruction maintenance means, and the machine instruction code read by said instruction read-out means and the machine instruction code held at said 1st instruction maintenance means, It is translation equipment for the information processor equipped with a selection means to output the machine instruction code which replaced with the machine instruction code read by said instruction read-out means when coincidence of a code was detected by said comparison means, and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which said machine instruction code generation means makes store said 2nd machine instruction code in said 1st instruction maintenance means, Translation equipment according to claim 2 characterized by generating the machine instruction code which makes said 1st machine instruction code store in said 2nd instruction maintenance means, preceding both with said 2nd machine instruction code, and stationing them.
[Claim 4] Said 2nd machine instruction code is translation equipment according to claim 3 characterized by being one of the machine instruction codes decoded as an undefined-instruction code by said decode means.
[Claim 5] Said frequency analysis means the train of the machine instruction code generated by said assemble means Divide that it is few into two groups of the 1st group and the 2nd group as this order performs, and it searches. In each group, a machine instruction code with the high frequency of occurrence is extracted as the 3rd machine instruction code and 4th machine instruction code. Said machine instruction code generation means While transposing said 3rd machine instruction code in said 1st group generated by said assemble means, and the 4th machine instruction code in said 2nd group to the 5th machine instruction code with the word length shorter than each machine instruction code The machine instruction code which makes said 1st instruction maintenance means store said 5th machine instruction code in the suitable part of said 1st group, Translation equipment according to claim 3 characterized by arranging the machine instruction code which makes said 3rd machine instruction code store in said 2nd instruction maintenance means, and arranging the machine instruction code which makes said 2nd instruction maintenance means store said 4th machine instruction code in the suitable part

of said 2nd group.
[Claim 6] Said 5th machine instruction code is translation equipment according to claim 5 characterized by being one of the machine instruction codes decoded as an undefined-instruction code by said decode means.
[Claim 7] The instruction read-out means which reads a machine instruction code from the storage which stores two or more machine instruction codes, A decode means to decode a machine instruction code, and an activation means to perform a machine instruction code according to said decode means, A 1st instruction maintenance means to save the 1st specific machine instruction code, and a 2nd instruction maintenance means to save the 2nd different specific machine instruction code from said 1st machine instruction code, It has a comparison means to detect coincidence with the machine instruction code read by said instruction read-out means, and said 1st machine instruction code saved for said 1st instruction maintenance means. Said decode means The information processor characterized by replacing with the machine instruction code read by said instruction read-out means, and decoding said 2nd machine instruction code saved for said 2nd instruction maintenance means when coincidence of a code is detected by said comparison means.
[Claim 8] Said 1st machine instruction code is an information processor according to claim 7 characterized by having the word length shorter than the word length of said 2nd machine instruction code.
[Claim 9] It is the information processor according to claim 8 characterized by performing gradually decode of said 2nd machine instruction code in said decode means considering the word length of said 1st machine instruction code as a unit.
[Claim 10] Said 1st machine instruction code is the information processor of nine claim 7 characterized by being one of the machine instruction codes decoded as an undefined-instruction code by said decode means thru/or given in any 1 term.
[Claim 11] An instruction read-out means, a decode means, the 1st instruction maintenance means, and the 2nd instruction maintenance means, A comparison means to detect coincidence with the machine instruction code read by said instruction read-out means, and the machine instruction code held at said 1st instruction maintenance means, When coincidence of a code is detected by said comparison means, with said instruction read-out means It is the record medium which stored the executive program performed by the information processor equipped with a selection means to output the machine instruction code which replaced with the read machine instruction code and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which makes the 1st specific machine instruction code store in said 1st instruction maintenance means, The record medium characterized by for said each of both machine instruction codes preceding with said 1st machine instruction code, and arranging them including the machine instruction code which makes the 2nd specific machine instruction code which has the word length longer than said 1st machine instruction code store in said 2nd instruction maintenance means.
[Claim 12] Said record medium contains the machine instruction code which makes the 3rd specific machine instruction code which has the word length longer than said 1st machine instruction code store in said 2nd instruction maintenance means. Said machine instruction code which makes the 2nd machine instruction code store in said 2nd instruction maintenance means Said machine instruction code which it precedes [code] with said 1st machine instruction code of the head in the specific group of said executive program, is arranged [code], and makes the 3rd machine instruction code store in said 2nd instruction maintenance means The record medium according to claim 11 characterized by preceding with said 1st machine instruction code of the head in other groups of said executive program, and being arranged.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the translation equipment which changes into the program of a machine instruction code the program written by the mnemonic, information processors including the microcomputer which performs the program of the machine instruction code on a target serially, and the record medium which records the executive program.
[0002]
[Description of the Prior Art] Without carrying out processing performance degradation of a microcomputer with large-scale-izing of a program size in recent years, instruction code size is compressed and it is necessary to decrease the storage capacity of a program.
[0003] Hereafter, the conventional information processor is explained.
[0004] Drawing 6 shows the configuration of the instruction code of the conventional information processor. In drawing 6 , the instruction codes 1 and 72 by which 71 is constituted only from an operation code of 8 bits of basic word length are the instruction codes 2 which consist of operation code section 72a with which two operation codes 1 and 2 of 8 bits of basic word length combined, and operand part 72b which consisted of 8-bit operands.
[0005] Here, operation code section 72a controls activation of each instruction, and the operation code of 8 bits of basic word length consists of at least one or more pieces. Operand part 72b is operation data which are needed in the case of activation of each instruction controlled by operation code section 72a, and the code of 8 bits of basic word length consists of one or more pieces. Each instruction code may consist of a case where it consists of only operation codes, and operation code section 72a and operand part 72b.
[0006] Drawing 7 is the block diagram showing the configuration of the conventional information processor. The bus to which a store (for example, ROM) for 62 to store a program code, the instruction decoder which decodes the instruction code which read 63 from the store 62 by 8 bitwises, the computing element which operates according to the instruction code from which 64 was decoded by the instruction decoder 63, and 65 transmit a microcode in drawing 7 , and 66 transmits an operation code, and 67 are buses to which an operand is transmitted.
[0007] And operation code section 72a of each instruction is beforehand mapped by the higher instruction of operating frequency so that the word length of the operation code section may become short.
[0008] Next, the actuation is explained about the information processor constituted like drawing 7 .
[0009] First, a user program is changed into instruction code and it stores in storage 62. An instruction decoder 63 decodes operation code section 72a which was beginning to read operation code section 72a one by one by 8 bitwises through the bus 66 from a store 62, and was outputted from the store 62 by 8 bitwises, and outputs the microcode 65 which controls actuation of a computing element 64 to a computing element 64.
[0010] A computing element 64 performs reception and predetermined actuation for the microcode 65 outputted from the instruction decoder 63, and operand part 72b outputted through a bus 67 from a store 62.

[0011]
[Problem(s) to be Solved by the Invention] However, with said conventional configuration, since the word length of the operation code section is determined by strictly average operating frequency, it is immobilization by instruction, and in the specific program for which reality uses a long instruction of the word length of the operation code section by high frequency since the operating frequency of an instruction differs for every program, the technical problem that code size became large occurred. Moreover, by one side, in order to make code size small, the technical problem that it was necessary to combine with the operating frequency of an instruction of such a specific program, and to remake an instruction decoder also occurred.
[0012] This invention does not solve such a conventional technical problem, and aims at offering the information processor and translation equipment which made it possible to assign the short word length's operation code section to the high instruction of operating frequency for every program, and its storage, without being accompanied by modification of an instruction decoder.
[0013]
[Means for Solving the Problem] In order to solve this technical problem and to attain the purpose the translation equipment of this invention An assemble means to be translation equipment which changes into the program of a machine instruction code the program written by the mnemonic, to input an instruction of a mnemonic notation, and to generate a corresponding machine instruction code, It is characterized by having the machine instruction code generation means which transposes the 1st specific machine instruction code of the inside generated by said assemble means to the 2nd machine instruction code with the word length shorter than said 1st machine instruction code.
[0014] Thereby, the 1st specific machine instruction code is transposed to the 2nd machine instruction code with the short word length.
[0015] Here, though said translation equipment searches further the train of the machine instruction code generated by said assemble means, is equipped with a frequency analysis means to extract a machine instruction code with the high frequency of occurrence and determines said 1st machine instruction code based on the result of the frequency analysis in said frequency analysis means, it is good.
[0016] Said translation equipment Furthermore, an instruction read-out means, a decode means, and the 1st instruction maintenance means, A comparison means to detect coincidence with the 2nd instruction maintenance means, and the machine instruction code read by said instruction read-out means and the machine instruction code held at said 1st instruction maintenance means, It is translation equipment for the information processor equipped with a selection means to output the machine instruction code which replaced with the machine instruction code read by said instruction read-out means when coincidence of a code was detected by said comparison means, and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which said machine instruction code generation means makes store said 2nd machine instruction code in said 1st instruction maintenance means, It is good, though the machine instruction code which makes said 1st machine instruction code store in said 2nd instruction maintenance means is generated, and both are preceded with said 2nd machine instruction code and stationed.
[0017] Here, though said 2nd machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good.
[0018] Said frequency analysis means or the train of the machine instruction code generated by said assemble means here Divide that it is few into two groups of the 1st group and the 2nd group as this order performs, and it searches. In each group, a machine instruction code with the high frequency of occurrence is extracted as the 3rd machine instruction code and 4th machine instruction code. Said machine instruction code generation means While transposing said 3rd machine instruction code in said 1st group generated by said assemble means, and the 4th machine instruction code in said 2nd group to the 5th machine instruction code with the word length shorter than each machine instruction code The machine instruction code which makes said 1st instruction maintenance means store said 5th machine instruction code in the suitable part of said 1st group, It is good, though the machine instruction code which makes said 3rd

machine instruction code store in said 2nd instruction maintenance means is arranged and the machine instruction code which makes said 2nd instruction maintenance means store said 4th machine instruction code in the suitable part of said 2nd group is arranged.
[0019] Thereby, the 3rd [of pinpointing in the 1st group] machine instruction code and the 4th specific machine instruction code in the 2nd group are transposed to the 5th machine instruction code with the respectively short word length.
[0020] Here, though said 5th machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good.
[0021] Moreover, an instruction read-out means by which the information processor of this invention reads a machine instruction code from the storage which stores two or more machine instruction codes, A decode means to decode a machine instruction code, and an activation means to perform a machine instruction code according to said decode means, A 1st instruction maintenance means to save the 1st specific machine instruction code, and a 2nd instruction maintenance means to save the 2nd different specific machine instruction code from said 1st machine instruction code, It has a comparison means to detect coincidence with the machine instruction code read by said instruction read-out means, and said 1st machine instruction code saved for said 1st instruction maintenance means. Said decode means When coincidence of a code is detected by said comparison means, it is characterized by replacing with the machine instruction code read by said instruction read-out means, and decoding said 2nd machine instruction code saved for said 2nd instruction maintenance means.
[0022] Thereby, the 1st machine instruction code is transposed to the 2nd machine instruction code, and is decoded.
[0023] Here, though said 1st machine instruction code has the word length shorter than the word length of said 2nd machine instruction code, it is good.
[0024] Furthermore, it is good though decode of said 2nd machine instruction code in said decode means is gradually performed considering the word length of said 1st machine instruction code as a unit.
[0025] In each above-mentioned information processor, though said 1st machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good.
[0026] The record medium of this invention Moreover, an instruction read-out means, a decode means, and the 1st instruction maintenance means, A comparison means to detect coincidence with the 2nd instruction maintenance means, and the machine instruction code read by said instruction read-out means and the machine instruction code held at said 1st instruction maintenance means, When coincidence of a code is detected by said comparison means, with said instruction read-out means It is the record medium which stored the executive program performed by the information processor equipped with a selection means to output the machine instruction code which replaced with the read machine instruction code and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which makes the 1st specific machine instruction code store in said 1st instruction maintenance means, It is characterized by for each both machine instruction code that described above the 2nd specific machine instruction code which has the word length longer than said 1st machine instruction code including the machine instruction code made to store in said 2nd instruction maintenance means preceding with said 1st machine instruction code, and arranging it.
[0027] Thereby, the 1st machine instruction code with the short word length is returned to the 2nd machine instruction code.
[0028] Said record medium contains the machine instruction code which makes the 3rd specific machine instruction code which has the word length still longer than said 1st machine instruction code store in said 2nd instruction maintenance means here. Said machine instruction code which makes the 2nd machine instruction code store in said 2nd instruction maintenance means Said machine instruction code which it precedes [code] with said 1st machine instruction code of the head in the specific group of said executive program, is arranged [code], and makes the 3rd machine instruction code store in said 2nd instruction maintenance means It is good, though it precedes with said 1st machine instruction code of the head in other groups of said executive

program and is arranged.
[0029] Thereby, the 1st machine instruction code with the short word length is returned to the 2nd machine instruction code in a specific group, and is returned to the 3rd machine instruction code in other groups.
[0030]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.
[0031] Drawing 1 is the block diagram of the translation equipment which changes into instruction code from the assembler program in the gestalt of operation of this invention. In drawing 1 , the assemble section into which 41 translates the assembler program storing section into, and 42 translates the assembler program of the assembler program storing section 41, the middle instruction code train storing section by which 43 is generated in the assemble section 42, the frequency analysis section from which 44 extracts the instruction frequency in the middle instruction code train storing section 43, the instruction frequency table storing section by which 45 was generated in the frequency analysis section 44, and 46 are the instruction code train storing section generated in the instruction code generation section and 47.
[0032] Drawing 2 shows the example of the translation equipment shown in drawing 1 of operation. As for the instruction code train by which an assembler program and 52 are generated for 51 and an instruction frequency table and 54 are generated for a middle instruction code train and 53, and 55, in drawing 2 , the data set instruction to Register A and 56 are the data set instructions to Register B.
[0033] Actuation of translation equipment is explained below using drawing 1 and drawing 2 .
[0034] First, based on the instruction code already assigned, in the assemble section 42, the assembler program 51 in the assembler program storing section 41 is translated into the middle instruction code train 52, and is stored in the middle instruction code train storing section 43. This is performed using a well-known technique.
[0035] Next, in the frequency analysis section 44, the extract of the frequency information on the instruction currently used in the middle instruction code train 52 in the middle instruction code train storing section 43 is performed, the instruction frequency table 53 is created, and it is stored in the instruction frequency table storing section 45. In this example, the table in which the operating frequency of instruction code "FF44" had the information that it was 2 times and the operating frequency of other instruction codes was 1 time is generated.
[0036] And in the instruction code generation section 46, "FF44" which is instruction code with high operating frequency is changed at the operation code in a reservation field "05" the middle instruction code train 52 and based on the instruction frequency table 53. And the data set instruction 56 which stores in 16 bits of high orders of Register B the long operation code "FF44" of the word length before the data set instruction 55 which stores the short operation code "05" of the word length after replacement in Register A, and replacement is generated, respectively, and the last instruction code train 54 is generated in the instruction code train storing section 47.
[0037] Drawing 3 is the bit allocation Fig. of an instruction of the information processor in the gestalt of operation of this invention, and, as for this, basic word length shows the 8-bit operation code section.
[0038] In drawing 3 , they are the reservation field whose word length of the operation-code section by which the instruction is not mapped of 21 is 8 bits, the extended instruction which the word length of the operation-code section shows that 22 is 8-bit instruction part and an instruction whose word length of the operation code section of 24-bit instruction part and 25 the word length of the operation-code section is [23 / for the word length of the operation code section] 16 bits as for 16-bit instruction part and 24, and the extended instruction in which it be shown that 26 is an instruction whose word length of the operation-code section is 24 bits.
[0039] By setting the instruction part 23 whose word length of the operation code section is 16 bits here to "FF" which shows that the 1st operation code is the extended instruction 25, the instruction part 24 which shows that the word length of the operation code section is 24 bits is

set to "FF" which shows that the 1st operation code is the extended instruction 25, and is set to "FF" which shows that the 2nd operation code is also the extended instruction 26.
[0040] Here, in drawing 3 , 16 "0F" are secured from "00", and, as for the reservation field 21, an operation code makes replacement of 16 operation codes possible. For example, within a program, the instruction "mov" (an operation code is "FF44") whose word length of the operation code section is 16 bits transposes to the operation code in the reservation field 21 "05", when operating frequency is high.
[0041] Drawing 4 is the block diagram of the information processor in the gestalt of operation of this invention. In drawing 4 , 11 is an instruction processing unit and consists of following each part. Namely, the 8-bit register A which stores the short operation code of the word length after replacement in case 12 replaces an operation code The 24-bit register B with which 13 stores the long operation code of the word length before replacement 14 is a comparator which outputs the control signal 16 with the operation code read from the store 62 via the bus 66, and the data in agreement stored in the register A12, and this control signal 16 controls a selector 15. The selector which 15 chooses one of the data stored in an output and a register B13 from the store 62, and is outputted, The sequencer by which 17 controls an instruction decode, the control signal with which 18 performs control of a register B13 and a selector 15, The bus which outputs the operation code by which 19 is stored in the register A12, the bus which outputs the operation code by which 110 is stored in the register B12, and 111 are buses by which the operation code chosen by the selector 15 is outputted.
[0042] In addition, a store 62, an instruction decoder 63 and a computing element 64, a microcode 65, a bus 66, and a bus 67 are the same configurations as usual (drawing 7).
[0043] The actuation of an information processor constituted as mentioned above is explained.
[0044] Drawing 5 shows the relation between a user's program and the instruction code at the time of being processed by the instruction decoder 63. In drawing 5 , 31 is the program code stored in the storage 62 in drawing 4 , and is the same as that of the instruction code train 54 of drawing 2 , and 32 is instruction code processed by the instruction decoder 63 in drawing 4 . A program code 31 is the case where the instruction "mov" which consists of two operation codes of the 8 bits of the basic word length "FF44" with high operating frequency, within the user program is mapped by the operation code "05" secured as a reservation field 21 in drawing 3 .
[0045] Hereafter, it explains taking the case of the case where activation of a program code 31 is performed.
[0046] An instruction processing unit 11 is read in order of "B0 of the program code 31 54 stored in storage 62, i.e., the instruction code train shown in drawing 2 ,", "05", "B1", "FF", "44", "30", "05", "31", "05", and "32."
[0047] First, it is outputted to the bus 66 to which an operation code "B0" transmits an operation code, and the comparison with the operation code "05" stored in the register A12 by the comparator 14 is performed, and since it is an inequality, a selector 15 outputs the operation code "B0" of a bus 66 to a bus 111. An instruction decoder 63 decodes the operation code "B0" of a bus 111, and outputs the microcode 65 which carries out the data set to a register A12 to a computing element 64. A computing element 64 sets data "05" to a register A12 according to the operand "05" outputted through the bus 67 to which an operand is transmitted from a store 62 according to the microcode 65 outputted from the instruction decoder 63.
[0048] Next, an operation code "B1" is outputted to 66, the comparison with an operation code "05" is performed by the comparator 14, and since it is an inequality, a selector 15 outputs the operation code "B1" of a bus 66 to a bus 111.
[0049] An instruction decoder 63 decodes the operation code "B1" of a bus 111, and outputs the microcode 65 which carries out the data set to a register B13 to a computing element 64. A computing element 64 performs the data set to a register B13 according to the microcode 65 outputted from the instruction decoder 63. First, the operand "FF" outputted through the bus 67 to which an operand is transmitted is received, it transposes to 8 bits of high orders of a register B13, and a front operation code "FF" is stored. Next, data "44" are set to 8 bits of media of a register B13 in response to an operand "44." Nothing is stored in 8 bits of low order of a register B13.

[0050] Next, an operation code "30" is outputted to a bus 66, the comparison with the operation code "05" stored in the register A12 by the comparator 14 is performed, and since it is an inequality, a selector 15 outputs the operation code "30" of a bus 66 to a bus 111.
[0051] An instruction decoder 63 decodes the operation code "30" of a bus 111, and outputs the microcode 65 which controls actuation of the instruction-processing-unit 11 interior to a computing element 64. A computing element 64 performs predetermined actuation defined as the operation code "30" according to the microcode 65 outputted from the instruction decoder 63.
[0052] Then, since an operation code "05" is outputted to a bus 66 and is in agreement from a store 62, a comparison is performed by the comparator 14, and a selector 15 chooses and outputs a register B13 side.
[0053] At this time, by control of a sequencer 17, a selector 15 outputs the code of "FF" of 8 bits of high orders of a register B13, then, outputs the code of "44" of 8 bits of media to an instruction decoder 63 first, to an instruction decoder 63, and performs predetermined actuation defined by the operation code "FF44" with a computing element 64.
[0054] Hereafter, decode of the instruction code of "31", "05", and "32" is performed one by one similarly, and actuation according to the instruction code 32 shown in drawing 5 is performed in the instruction-processing-unit 11 interior.
[0055] According to the gestalt of this operation, it becomes possible to make small program code size of the instruction code train 54 generated by assemble equipment as mentioned above by transposing "mov" and the operation code "FF44" which are the instruction with the high operating frequency in an assembler program 51 to the operation code in the reservation field 21 "05." Moreover, in order to decode by transposing an operation code "05" to an operation code "FF44" inside an information processor, it is not accompanied by modification of an instruction decoder 63.
[0056] In addition, although the 16-bit operation code "FF44" was transposed to the 8-bit operation code "05", the operation code "05" was stored in the register A12, the operation code "FF44" was stored in the register B13 and decode of a deed instruction was replaced inside the information processor in the information processor of the gestalt of the above-mentioned implementation, it can also make it the same to transpose a 24-bit operation code to a 8-bit operation code.
[0057] Moreover, although the register A12 was 8-bit width of face, it is good as for 16-bit width of face. By carrying out like this, it becomes possible to transpose a 24-bit operation code to a 16-bit operation code.
[0058] Moreover, although the number of a register A12 and registers B13 was one, they may be prepared two or more pairs. By carrying out like this, replacement of two or more instruction codes becomes possible.
[0059] Moreover, although the frequency analysis section 44 searches all the middle instruction code trains stored in the middle instruction code train storing section 43 with the assemble equipment shown in drawing 1 of the gestalt of the above-mentioned operation and instruction code with the highest frequency is extracted A middle instruction code train is divided into some groups, and you may make it insert the instruction which sets to a register B13 the instruction code which extracted instruction code with high frequency and was further extracted into the head part of each group in the instruction code generation section 46 in each. When locality is in the frequency of an instruction in a middle instruction code train by carrying out like this, or when locality can be given positively, the instruction code from which plurality differs can be transposed to one instruction code with the short word length, and each can be returned.
[0060] Moreover, the executive program stored in the instruction code train storing section 47 may record semiconductor memory media, such as optical disk media, such as magnetic-disk media, such as a floppy disk, and CD-ROM, and a flash memory, etc. on the record medium which can be read by computer.
[0061]
[Effect of the Invention] So that clearly from the above explanation the translation equipment of this invention An assemble means to be translation equipment which changes into the program of a machine instruction code the program written by the mnemonic, to input an instruction of a

mnemonic notation, and to generate a corresponding machine instruction code, It is characterized by having the machine instruction code generation means which transposes the 1st specific machine instruction code of the inside generated by said assemble means to the 2nd machine instruction code with the word length shorter than said 1st machine instruction code.
[0062] Thereby, the 1st specific machine instruction code is transposed to the 2nd machine instruction code with the short word length, and can assign the short word length's machine instruction code to a specific machine instruction code for every program.
[0063] Here, though said translation equipment searches further the train of the machine instruction code generated by said assemble means, is equipped with a frequency analysis means to extract a machine instruction code with the high frequency of occurrence and determines said 1st machine instruction code based on the result of the frequency analysis in said frequency analysis means, it is good.
[0064] A machine instruction code with the high frequency of occurrence can be replaced by this, and much more reduction of code size is attained.
[0065] Said translation equipment Furthermore, an instruction read-out means, a decode means, and the 1st instruction maintenance means, A comparison means to detect coincidence with the 2nd instruction maintenance means, and the machine instruction code read by said instruction read-out means and the machine instruction code held at said 1st instruction maintenance means, It is translation equipment for the information processor equipped with a selection means to output the machine instruction code which replaced with the machine instruction code read by said instruction read-out means when coincidence of a code was detected by said comparison means, and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which said machine instruction code generation means makes store said 2nd machine instruction code in said 1st instruction maintenance means, It is good, though the machine instruction code which makes said 1st machine instruction code store in said 2nd instruction maintenance means is generated, and both are preceded with said 2nd machine instruction code and stationed.
[0066] Here, though said 2nd machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good.
[0067] Said frequency analysis means or the train of the machine instruction code generated by said assemble means here Divide that it is few into two groups of the 1st group and the 2nd group as this order performs, and it searches. In each group, a machine instruction code with the high frequency of occurrence is extracted as the 3rd machine instruction code and 4th machine instruction code. Said machine instruction code generation means While transposing said 3rd machine instruction code in said 1st group generated by said assemble means, and the 4th machine instruction code in said 2nd group to the 5th machine instruction code with the word length shorter than each machine instruction code The machine instruction code which makes said 1st instruction maintenance means store said 5th machine instruction code in the suitable part of said 1st group, It is good, though the machine instruction code which makes said 3rd machine instruction code store in said 2nd instruction maintenance means is arranged and the machine instruction code which makes said 2nd instruction maintenance means store said 4th machine instruction code in the suitable part of said 2nd group is arranged.
[0068] this transposes the 3rd [of pinpointing in the 1st group] machine instruction code, and the 4th specific machine instruction code in the 2nd group to the 5th machine instruction code with the respectively short word length -- having -- every program -- and the short word length's machine instruction code can be assigned to a specific machine instruction code with the high frequency of occurrence for every group divided or more into two, and contraction of much more code size can be aimed at.
[0069] Here, though said 5th machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good.
[0070] Moreover, an instruction read-out means by which the information processor of this invention reads a machine instruction code from the storage which stores two or more machine instruction codes, A decode means to decode a machine instruction code, and an activation means to perform a machine instruction code according to said decode means, A 1st instruction

maintenance means to save the 1st specific machine instruction code, and a 2nd instruction maintenance means to save the 2nd different specific machine instruction code from said 1st machine instruction code, It has a comparison means to detect coincidence with the machine instruction code read by said instruction read-out means, and said 1st machine instruction code saved for said 1st instruction maintenance means. Said decode means When coincidence of a code is detected by said comparison means, it is characterized by replacing with the machine instruction code read by said instruction read-out means, and decoding said 2nd machine instruction code saved for said 2nd instruction maintenance means.
[0071] Thereby, the 1st machine instruction code is transposed to the 2nd machine instruction code, is decoded, and does not need modification of a decode means.
[0072] Here, though said 1st machine instruction code has the word length shorter than the word length of said 2nd machine instruction code, it is good.
[0073] Furthermore, it is good though decode of said 2nd machine instruction code in said decode means is gradually performed considering the word length of said 1st machine instruction code as a unit.
[0074] Though said 1st machine instruction code is one of the machine instruction codes decoded as an undefined-instruction code by said decode means, it is good. [of each above-mentioned information processor]
[0075] An operation of the 2nd machine instruction code is acquired by these in 1st machine instruction code with the word length shorter than it.
[0076] The record medium of this invention Moreover, an instruction read-out means, a decode means, and the 1st instruction maintenance means, A comparison means to detect coincidence with the 2nd instruction maintenance means, and the machine instruction code read by said instruction read-out means and the machine instruction code held at said 1st instruction maintenance means, When coincidence of a code is detected by said comparison means, with said instruction read-out means It is the record medium which stored the executive program performed by the information processor equipped with a selection means to output the machine instruction code which replaced with the read machine instruction code and was held at said 2nd instruction maintenance means to said decode means. The machine instruction code which makes the 1st specific machine instruction code store in said 1st instruction maintenance means, It is characterized by for each both aforementioned machine instruction code preceding with said 1st machine instruction code, and arranging it including the machine instruction code which makes the 2nd specific machine instruction code which has the word length longer than said 1st machine instruction code store in said 2nd instruction maintenance means.
[0077] Thereby, the 1st machine instruction code with the short word length is returned to the 2nd machine instruction code, and can assign the short word length's machine instruction code to a specific machine instruction code for every program.
[0078] Said record medium contains the machine instruction code which makes the 3rd specific machine instruction code which has the word length still longer than said 1st machine instruction code store in said 2nd instruction maintenance means here. Said machine instruction code which makes the 2nd machine instruction code store in said 2nd instruction maintenance means Said machine instruction code which it precedes [code] with said 1st machine instruction code of the head in the specific group of said executive program, is arranged [code], and makes the 3rd machine instruction code store in said 2nd instruction maintenance means It is good, though it precedes with said 1st machine instruction code of the head in other groups of said executive program and is arranged.
[0079] thereby, the 1st machine instruction code with the short word length is returned to the 2nd machine instruction code in a specific group, and is returned to the 3rd machine instruction code in other groups -- having -- every program -- and the short word length's machine instruction code can be assigned to a specific machine instruction code with the high frequency of occurrence for every group divided or more into two.
[0080] The practical value of the technique of this invention is large as mentioned above.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram of the translation equipment in the gestalt of operation of this invention
[Drawing 2] Drawing having shown the example of the translation equipment of drawing 1 of operation
[Drawing 3] The bit allocation Fig. of an instruction of the information processor in the gestalt of operation of this invention
[Drawing 4] The block diagram showing the configuration of the information processor in the gestalt of operation of this invention
[Drawing 5] Drawing having shown relation with the instruction code at the time of being processed with the user program code of an information processor and information processor in the gestalt of operation of this invention
[Drawing 6] The block diagram of the instruction code of the conventional information processor
[Drawing 7] The block diagram showing the configuration of the conventional information processor
[Description of Notations]
11 Instruction Processing Unit
12 Register A
13 Register B
14 Comparator
15 Selector
16 18 Control signal
17 Sequencer
19,110,111 Bus
21 Reservation Field
22 Instruction Part whose Operation Code is 8 Bits
23 Instruction Part whose Operation Code is 16 Bits
24 Instruction Part whose Operation Code is 24 Bits
31 Program Code
32 Instruction Code Processed Inside
41 Assembler Program Storing Section
42 Assemble Section
43 Middle Instruction Code Train Storing Section
44 Frequency Analysis Section
45 Instruction Frequency Table Storing Section
46 Instruction Code Generation Section
47 Instruction Code Train Storing Section
51 Assembler Program
52 Middle Instruction Code Train
53 Instruction Frequency Table
54 Instruction Code Train

55 Data Set Instruction to Register A
56 Data Set Instruction to Register B
62 Storage
63 Instruction Decoder
64 Computing Element
65 Microcode
71 Instruction Code 1
72 Instruction Code 2

[Translation done.]